Enhancement Mode Antimonide Quantum Well MOSFETs with High Electron Mobility and GHz Small-Signal Switching Performance

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***Abstract*—This paper demonstrates, for the first time, enhancement mode antimonide MOSFETs by integrating a composite high-κ gate stack (3nm Al_2O_3-1nm GaSb) with ultra-thin $InAs_{0.7}Sb_{0.3}$ QW (7.5nm). The MOSFET exhibits record high electron drift mobility of 5200 cm^2/Vs at a carrier density (N_s) of $1.8x10^{12}cm^{-2}$, sub-threshold slope of 150mV/decade, I_{ON}-I_{OFF} ratio of ~4000x within a voltage window of ~1V, high I_{ON} of 40μA/μm at V_{DS} of 0.5V for 5μm gate length (L_G) device. The device exhibits excellent pinch-off in the output characteristics with no evidence of impact ionization enabled by enhanced quantization and e-mode operation. RF characterization allows extraction of the intrinsic device metrics (C_{gs}, C_{gd}, g_m, g_{ds}, v_{eff}, and f_t) and the parasitic resistive and capacitive elements limiting the short channel device performance.**

***Index Terms*—Antimonide MOSFET, InAsSb, high-κ dielectric, low power logic**

I. Introduction

DEPLETION mode $InAs_{0.8}Sb_{0.2}$ quantum well (QW) MOSFETs with high drive current have already been demonstrated [1], albeit with degraded I_{ON}-I_{OFF} ratio due to the accumulation of holes in the barrier layer. The device is suspectible to the hole accumulation problem due to the very high conduction band offset between the $InAs_{0.8}Sb_{0.2}$ quantum well and the InAlSb barrier layer. For ultra-low power logic devices, enhancement mode (e-mode) operation is required along with high I_{ON} and I_{ON}-I_{OFF} ratio over a limited gate voltage swing. In this paper, we demonstrate $InAs_{0.7}Sb_{0.3}$ QW MOSFETs with thin barrier and quantum well thickness which exhibits e-mode operation due to stronger quantum confinement effects [2, 3]. The scaling of the InAlSb barrier layer prevents hole accumulation during device turn-off, resulting in significantly improved I_{ON}-I_{OFF} ratio of 4000x at room temperature, which is a remarkable improvement over the previous generation thick QW device in [1] which had I_{ON}-I_{OFF} ratio of only 30x. Record high long channel electron mobility, short channel electron velocity (after series resistance correction) and GHz domain small-signal performance are also demonstrated in these e-mode $InAs_{0.7}Sb_{0.3}$ QW MOSFETs, for the first time.

The paper is organized as follows. Section II describes the device layer design and characterization, Section III describes

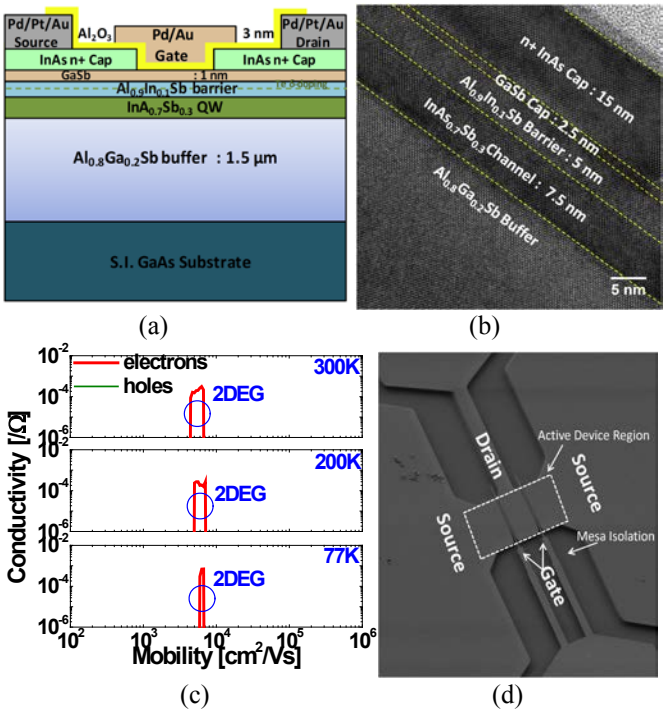

Fig. 1. (a) Schematic of the QW device structure. (b) TEM image of $InAs_{0.7}Sb_{0.3}$ QW stack with GaSb cap. GaSb cap enables dielectric integration [4], and the n+ InAs cap is used to improve access resistance (c) Quantitative Mobility Spectrum Analysis (QMSA) of $InAs_{0.7}Sb_{0.3}$ QW heterostructure layers showing single dominant electron conductivity peak, indicating no parallel conduction in the barrier or buffer layer. (d) Top view SEM image of the $InAs_{0.7}Sb_{0.3}$ QW-MOSFET with L_G=150nm.

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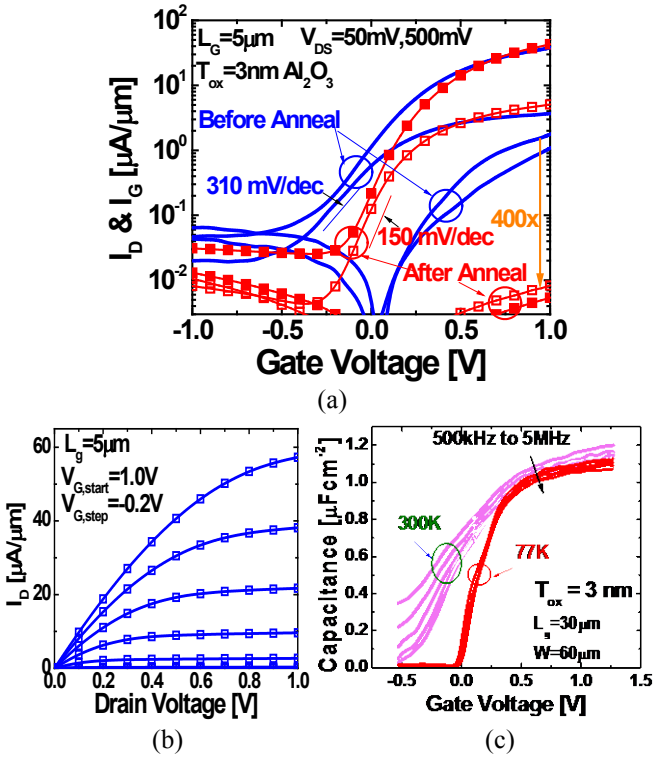

Fig. 2. (a) Transfer characteristics of the L_G=5μm device. (b) Output characteristics of L_G=1μm device, showing very good saturation without any effects of impact ionization. (c) Split C-V characteristics at 77K and 300K.

the DC and AC characteristics of the device, Section IV describes the RF characterization, followed by conclusions in Section V.

II. Device Layer Design and Characterization

Fig. 1(a) shows the schematic of the quantum well device structure. The quantum well is undoped and the $Al_{0.9}In_{0.1}Sb$ barrier layer has been doped ($2x10^{12}/cm^2$ Te) to provide carriers to the access regions. Fig. 1(b) shows the TEM micrographs of the $InAs_{0.7}Sb_{0.3}$ QWFET stack grown on GaAs by MBE and the defect free active device layers. Fig. 1(c) shows the quantitative mobility spectrum analysis (QMSA) for the QW heterostructure obtained using magneto conductance measurements at various temperatures and under varying magnetic field. There is a single dominant conductivity peak due to electrons indicating no parasitic or parallel conduction through the barrier or the metamorphic buffer layers. We obtain a room temperature Hall mobility of 5,500 cm^2/Vs (N_s=$1.8x10^{12}/cm^2$) for the QW heterostructure. Fig. 1(d) shows the top view SEM of the $InAs_{0.7}Sb_{0.3}$ MOS QWFET with 150nm L_G and composite high-κ gate stack (1nm GaSb-3nm Al_2O_3). Pd/Pt/Au metal stack was alloyed to form embedded contacts making direct ohmic contact with the QW. Device isolation was done using Cl_2/Ar based reactive ion etching (RIE) followed by 3nm thick Al_2O_3 deposition employing plasma enhanced ALD (PEALD) [4]. The device layers were treated in HCl (1HCl: $1H_2O$) for 30 sec prior to gate dielectric deposition. Pd/Au gate metal was defined using e-beam

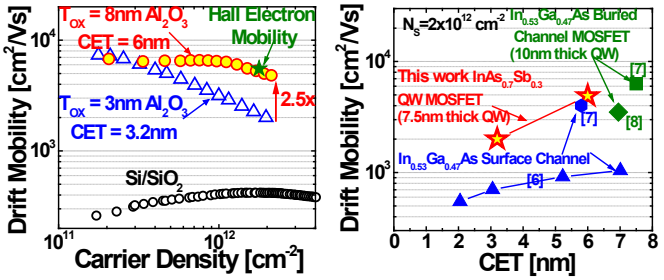

Fig. 3. (a) Electron drift mobility as a function of carrier density showing 2.5x enhancement on scaling oxide thickness. Record high electron mobility of 5200 cm^2/Vs achieved for the device with 8nm oxide at N_s=$1.8x10^{12}cm^{-2}$. (b) Electron drift mobility as a function of CET for the thin QW device (CET is obtained from split C-V and it includes semiconductor capacitance).

lithography and lift off process. The devices received a 10min post deposition anneal (PDA) at 180C in N_2 ambient to densify the dielectric and reduce the interface and bulk defects.

III. DC and AC Characterization

Fig. 2(a) shows the effect of N_2 anneal on the transfer characteristics of the fabricated device. The sub-threshold slope (SS) improves to 150mV/dec after anneal from 310mV/dec before anneal, while the gate leakage reduces by ~400x after anneal. Fig. 2(b) shows the output characteristics of L_G=1μm devices which shows excellent saturation without any effect of impact ionization. High drain to source on-current of 40μA/μm is obtained for the L_G=5μm device at drain bias of 0.5V. The short channel devices, however, suffer from high access resistance (from undercut of the InAs cap) which limits the ON-current. Fig. 2(c) shows the split C-V characteristics of the thin QW device with 3nm Al_2O_3-1nm GaSb at 77K and 300K. The interface state density in these devices is $6x10^{12}cm^{-2}eV^{-1}$ obtained from the conductance analysis. Fig. 3(a) shows the effective electron drift mobility as a function of N_s. Interface charge contribution to the total charge density is corrected using the split C-V and simulated C-V [5]. Record high effective electron drift mobility of 5200 cm^2/Vs was achieved at N_s of $1.8x10^{12}cm^{-2}$, close to the Hall mobility of 5500 cm^2/Vs at the same N_s. Effective electron drift mobility as a function of the Capacitive Equivalent Thickness (CET) is shown in Fig. 3(b). A 2.5x improvement in the mobility was obtained on increasing the oxide thickness from 3nm to 8nm, indicating that the dominant scattering mechanism is due to fixed charge at the Al_2O_3-GaSb interface or metal-Al_2O_3 interface.

IV. RF Characterization

Limited data exist in literature till date on high frequency characterization of III-V quantum well FETs with integrated high-κ dielectric. RF characterization allows extraction of the intrinsic device metrics (C_{gs}, C_{gd}, g_m, g_{ds}, v_{eff}, and f_t) and the parasitic resistive and capacitive elements limiting the short channel device performance. The S-parameters of the device under test and the open and short dummy structures are

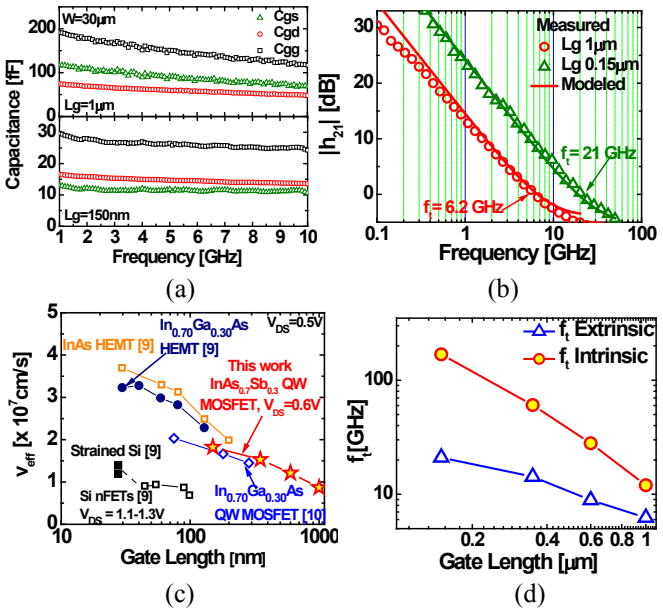

Fig. 4. (a) C_{gs} , C_{gd} and C_{gg} as a function of frequency for L_G=150nm and 1μm. High values of parasitic C_{gd} in these devices (due to incomplete isolation etch) limit RF performance, which could not be de-embedded during open calibration process. (b) Measured and modeled $|h_{21}|$ as a function of frequency. (c) Extracted intrinsic v_{eff} vs gate length showing v_{eff}=1.8x10^7 cm/s for 150nm L_G, one of the highest effective velocities reported for III-V devices. (d) Intrinsic and extrinsic f_t vs gate length.

measured. S-parameters of the device are obtained after the open-short de-embedding to remove the parasitic resistance and capacitance. From the de-embedded S-parameters of the device C_{gs}, C_{gd}, g_m, g_{ds} are obtained. Fig. 4(a) shows the C_{gs} , C_{gd} and C_{gg} as a function of frequency for L_G=150nm and 1μm. The de-embedded S-parameters of the device are modeled using an equivalent small signal model to extract the intrinsic device parameters, using the evaluated C_{gs}, C_{gd}, g_m, and g_{ds}. Fig. 4(b) shows the measured and the modeled $|h_{21}|$ versus frequency for L_G=150nm device (f_t, extrinsic= 21GHz) and L_G=1μm device (f_t, extrinsic= 6.5GHz) from 100MHz to 20GHz, which provides an excellent fit. High values of parasitic C_{gd} in these devices (due to incomplete isolation etch) limit the RF performance, which could not be de-embedded during the open calibration process. For the 150 nm L_G device, C_{gd} exceeds C_{gs} which limits the effective velocity (v_{eff}) and the cutoff frequency, f_t.

Fig. 4(c) shows the extracted source injection velocity ($v_{eff} = g_{mi}/slope(C_{gs}\ vs\ L_G)$, where g_{mi} is the intrinsic transconductance of the device) for different gate length devices. The device with 150nm L_G has a v_{eff} of 1.8x10^7 cm/s, one of the highest reported for III-V MOSFETs. Fig. 4(d) shows the intrinsic and extrinsic f_t vs L_G ($f_t = v_{eff}/2\pi L_G$). The intrinsic f_t is 160GHz for the 150nm device and 12GHz for the 1um device.

V. Conclusions

E-mode $InAs_{0.7}Sb_{0.3}$ QW MOSFETs has been demonstrated for the first time with record high effective electron drift mobility of 5200 cm^2/Vs at (N_s) of 1.8x10^{12}cm^{-2}, sub-threshold slope of 150mV/dec, and I_{ON}-I_{OFF} ratio of ~4000x within a voltage window of ~1V. Record high short channel electron velocity of 1.8x10^7 cm/s (after series resistance correction) and intrinsic f_t of 160GHz (extrinsic f_t of 21GHz, limited by parasitic capacitance and resistance) are reported in 150nm L_G device, for the first time.

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